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A verilog HDL based Implementations for quasi orthogonal space time block codes

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Abstract
STBC (Space Time Block Code) schemes are the most commonly used scheme in Multi Input and output Communication Systems for efficient data transmission and reception. In this paper we have more concentrated on the orthogonally of signals for more accurate data transmission. Here we have implemented the system assuming Quasi Orthogonal environmental as it is very suitable for more than two transmit antenna systems. Also in our previous paper we have demonstrated QOSTBC (Quasi Orthogonal STBC) lowers decoding complexity and in general higher BER performance is achieved. Our implementations has been synthesized and simulated using Xilinx ISE and coded with Verilog HDL.

Keywords: STBC, Xilinx ISE, QO OSTBC, Verilog HDL.

1. Introduction

QO-STBC

Currently diversity in the communications has been gained a method of analyzing effects of wireless fading channels because of its simplicity and feasibility of having multiple antennas at the base station. Quasi Orthogonal space–time block coding is an efficient approach towards achieving full diversity using basic Encoding and decoding techniques. This new architecture uses the concept of orthogonal designs for allowing maximum possible transmission rate and lower delay time. The focus of our study is to design a VLSI based architecture for designing Transmitter, Reciver and Comminicational channel with Verilog HDL coding paradism. Xilinx ISE simulator is used to simulate the design written in Verilog HDL language. Xilinx tool is used fast simulation of the design and it enables development and verification of the design completely. Verilog HDL is a language is used for describing digital electronic system. It arose out of the Gateway Automation Company in 1970's later owned by Cadence Systems, World's largest Semiconductor Company.
For this dissertation, we use Xilinx ISE design suite 9.1. We may generate synthesizable design in VHDL and Verilog languages. The Xilinx ISE design suite has several elements inbuilt such as counters, adders, multipliers, distributed ram, and block ram etc. These elements are fast and have low hardware requirements i.e. operation of these elements are fast and number of slices utilizes is less. Xilinx ISE design suite enables the user to know about the area utilized by the synthesizable design, maximum clock frequency supported by design, worst path delay in design etc. We can also analyse the RTL level design generated by the HDL design.
This XILINX release has been used for synthesis and simulations implementation of our design. We may also download any design or place and route the design on the desired FPGA after successfully verifying the synthesis and simulation results.

2. Proposed Method

Alamouti Codes

To demonstrate STBC (Space Time Block Codes), the Alamouti code, the very basic and commonly used space time code is explained in details.
Below figure represents an Alamouti code for two transmitters and one receiver system (2x1)

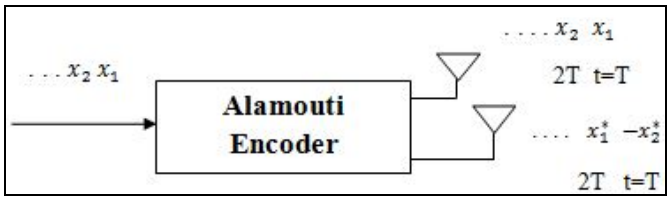

Fig 1: Alamouti encoder

h1 and h2 are impulse responses of the two channels whose envelopes follow Rayleigh distribution.

	Transmitter1	Transmitter2
Time t	x1	x2
Time t+T	-x2*	x1*

Where x1, x2 are the modulated symbols.
The received vectors are
y1= h1(x1) + h2(x2) +n1 (first time slot)
y2= h1(-x2*) + h2(x1*) +n2 (second time slot)
where n1,n2 denote AWGN noise and y1,y2 denote the received vectors

These equations may be written as

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} h_1 & h_2 \\ h_2^* & -h_1^* \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} n_1 \\ n_2 \end{bmatrix}$$

$$H = \begin{bmatrix} h_1 & h_2 \\ h_2^* & -h_1^* \end{bmatrix}$$

Is an 2×2 channel matrix
Or

Y = hx + n
and h is an orthogonal matrix

Decoding Scheme

Decoding is the process of converting received messages into codewords of a given code. There have been many methods of mapping messages into codewords. These are mostly used to regain messages sent over a noisy channel.
ML (Maximum Likelihood Decoding) algorithm is always assumed to be a low complex method for OSTBC (Orthogonal space-time block codes (OSTBCs) based on the real-valued lattice representation.

3. Simulation Results

Implementations for QOSTBC Encoder in Xilinx ISE

The scheme has been converted in verolig HDL code. Finally, for the bitstream conversion, the Xilinx ISE tool has used.

RTL Schematic for the Encoder

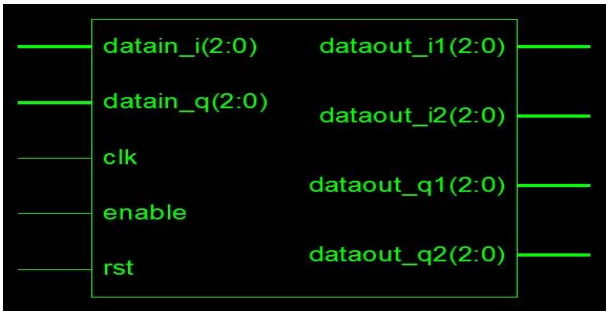

Fig 2: QO-STBC Encoder

The above RTL schematic represents, inputs to the QO-STBC encoder (datain_i1[2:0],datain_q1[2:0],a global clock input for synchronous operation of the decoder, enable and rst signals as additional inputs for activation of the block. The results of the block (dataout_i1[2:0], dataout_i2[2:0], dataout_q1[2:0], dataout_q2[2:0]) are considered as outputs.

RTL Schematic for Communication Channel

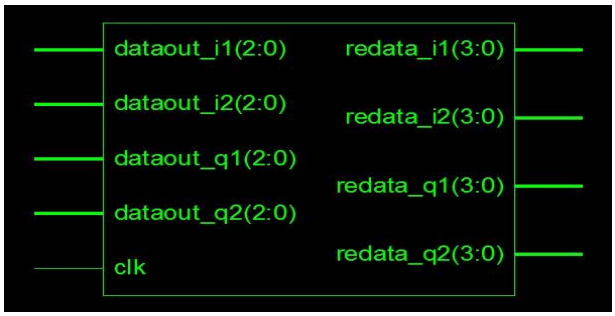

Fig 3: QO-STBC Communication Channel

The above RTL schematic represents, four channel coefficients as inputs (dataout_i1[2:0], dataout_i2[2:0], dataout_q1[2:0], dataout_q2[2:0]), a global clock input for synchronous operation of the decoder. The results of the block redata_i1[3:0], redata_i2[3:0], redata_q1[3:0], redata_q1[3:0] are considered as outputs.

RTL Schematic for Decoder

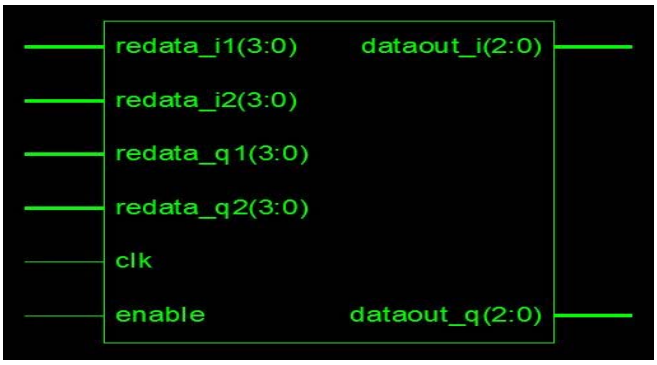

Fig 4: QO-STBC Decoder

The above RTL schematic represents, four channel coefficients as inputs (redata_i1[3:0], redata_i2[3:0], redata_q1[3:0], redata_q1[3:0]), a global clock input for synchronous operation of the decoder and enable signal input for activating the block. The results of the block dataout_1[2:0] and dataout_1[2:0] are considered as outputs.

Algorithm for the Virtual Relay Operation for Distributed QO-STBC Operations in Xilinx ISE

```
if (Input>=16'h1B && Previous Input>=16'h1B)
Count Value <= Count Value + 1;
else
Count Value <= 5'b00000;
end
if (Count Value > 5'b10100)
begin
Relay Out <= 1'b1;
end
else
begin
Relay Out <= 1'b0;
end
end
```

Device utilization summary for the QO-STBC Encoder

Selected Device:	3s50pq208-4
Number of Slices:	21 out of 768 2%
Number of Slice Flip Flops:	37 out of 1536 2%
Number of 4 input LUTs:	14 out of 1536 0%
Number of IOs:	21
Number of bonded IOBs:	20 out of 124 16%
Number of GCLKs:	1 out of 8 12%

Device utilization summary for QO-STBC Channel:

Selected Device:	3s50pq208-4
Number of Slices:	24 out of 768 3%

Number of Slice Flip Flops:	8 out of 1536 0%
Number of 4 input LUTs:	44 out of 1536 2%
Number of IOs:	29
Number of bonded IOBs:	29 out of 124 23%
IOB Flip Flops:	16
Number of GCLKs:	1 out of 8 12%

Device utilization summary for QO-STBC Decoder:

Selected Device:	3s50pq208-4
Number of Slices:	81 out of 768 10%
Number of Slice Flip Flops:	83 out of 1536 5%
Number of 4 input LUTs:	10 out of 1536 7%
Number of IOs:	24
Number of bonded IOBs:	24 out of 124 19%
Number of GCLKs:	1 out of 8 12%

Gate Net

Cell: in->out fanout Delay Delay Logical Name (Net Name)

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FDE: C->Q 1 0.720 0.801 dataout_i_2 (dataout_i_2)

OBUF: I->O 5.644 dataout_i_2_OBUF (dataout_i<2>)

Total 7.165ns (6.364ns logic, 0.801ns route)
(88.8% logic, 11.2% route)

Simulation Results for the QOSTBC Encoder

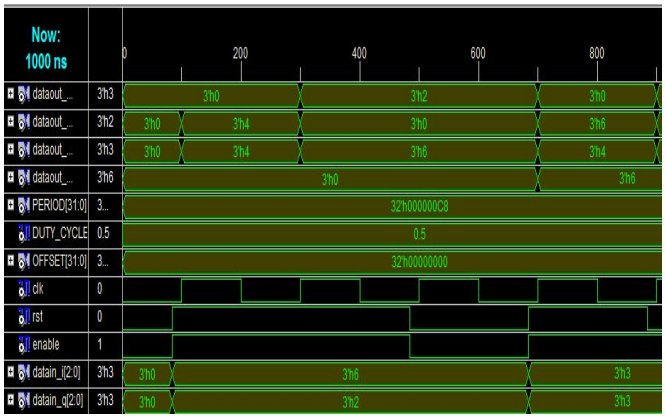

Fig 5: Simulation results for QO-STBC Encoder

Simulation Results for the QOSTBC Channel

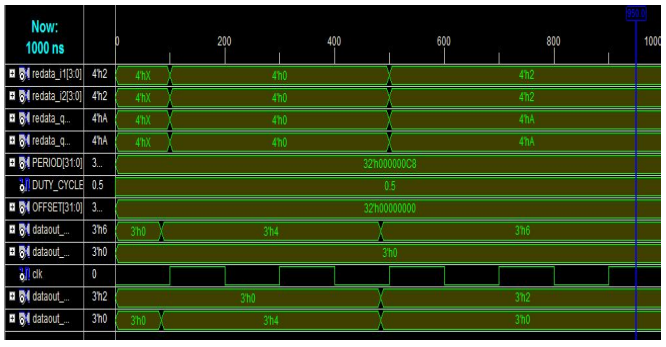

Fig 6: Simulation results for QO-STBC Channel

Simulation Results for the QOSTBC Decoder

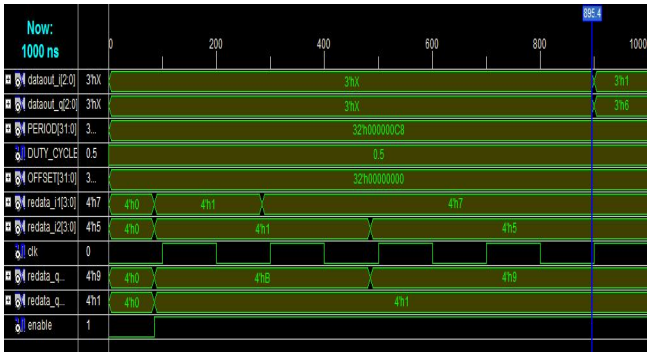

Fig 7: Simulation results for QO-STBC Decoder

IV. Conclusion

The prime focus of the Quasi orthogonal space time block code is to gain low complexity transmission and reception under fading channels. For considering the feasibility and practicability of the QO-STBC process, we have synthesized and Simulated the system in Verilog HDL language which is mostly used in semiconductor industries for design and verification methodology. Our results including RTL schematics and Device utilizations summary in virtual FPGA boards with no. of Flip flops, slices, Delay time represents, the system is efficient and may be used for hardware implementations. In future works our system may be modified for achieving higher transmission and reception rates, also n-Phase shift keying scheme may be adopted for better results.

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